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VLSI Circuits, 1993. Digest of Technical Papers. 1993 Symposium on , May 19-1993

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Solid-State Circuits, IEEE Journal of , Volume: 29 Issue: 4 , April 1994

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2 Memory array architecture and decoding scheme for 3V only sector erasable DINOR flash memory

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4 A 3.42 /spl mu/m/sup 2/ Flash Memory Cell Technology Conformable Sector Erase

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